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Thank you for being here..The problem of the brain in the status epilepticus. A central problem in the management of the status epilepticus is a reliable estimate of the extent of brain damage that may result from the prolonged disease. This paper reviews recent concepts of the pathophysiological sequelae of status epilepticus (i.e. brain dysfunction or injury) in order to identify those that may lead to better therapies. Brain dysfunction may be due to the seizure itself, direct metabolic effects or the spread of epileptiform activity or to effects of the seizure on the brain resulting from the compromised and dysfunctional cerebral circulation. The mechanisms of brain damage in the status epilepticus, either due to direct metabolic effects or to possible secondarily deranged brain function due to the compromised circulation, are not well understood. Changes in neurotransmitter function have been reported in rats following status epilepticus and in man following prolonged seizures. The autonomic disturbances which are seen after prolonged seizures may be a manifestation of these functional changes. Brain damage may take several forms. First, the prolonged seizure activity might be accompanied by focal infarction of the brain. Second, there may be a spread of the epilepsy to involve all parts of the brain. Third, there might be a persistent seizure suppression which prevents spread of the epileptiform discharge. There is some evidence that status epilepticus can have lasting effects on the brain. Careful evaluation of these effects may be important if they alter seizure thresholds or modify the threshold for further seizure activation. For example, post-status epilepticus psychosis might lead to a lowered seizure threshold which could be clinically important.

Management of the status epilepticus requires careful and repeated evaluation of the brain to determine the full extent of brain injury.Slideshare uses cookies to improve functionality and performance, and to provide you with relevant advertising. If you continue browsing the site, you agree to the use of cookies on this website. See our User Agreement and Privacy Policy. Slideshare uses cookies to improve functionality and performance, and 1cdb36666d

. Samsung 20MP Xpress q6 Chromebox (Chromebook) WiFi / Bluetooth. ForumÂ . Adobe Flash PlayerÂ . Samsung 40KS7050P Smart TV Compact Freeview HD Smart Tv Tvware. Freeview HD Player and DVB-T. Free USB-STICK 5032 download. bmm ht2105 manual ugarte.1. Field of the Invention The present invention relates to a semiconductor memory device. 2. Description of the Background Art In a conventional semiconductor memory device using MOS transistor as a memory element, it is generally difficult to increase storage capacitance and hence the size of capacitor must be reduced. This problem is particularly serious in 256M- and 1Gbit-DRAMs. In the 256M-DRAM, since an area available for capacitor is restricted, the dynamic random access memory (referred to as DRAM, hereinafter) of an stacked capacitor type is selected in order to enhance the storage capacitance. However, in the DRAM of the stacked capacitor type, since a capacitor portion is connected to a gate electrode or source electrode of a transfer transistor via a capacitor insulating film and a side wall structure is formed at the sides of a gate electrode, it is difficult to reduce the area of the memory cell. To increase the area available for capacitor, a DRAM of a trench type having a cylinder shape has been proposed. According to this DRAM, since a trench is formed in a semiconductor substrate and a capacitor element is disposed therein, the area available for capacitor is increased and thus the storage capacitance is enhanced. FIGS. 29 to 32 are cross-sectional views showing a conventional semiconductor memory device. Referring to FIG. 29, an element isolating oxide film 2 is formed on a semiconductor substrate 1 and a pad oxide film 4 is formed on the element isolating oxide film 2. On the pad oxide film 4, a control gate electrode 6 is formed and on the control gate electrode 6, a first inter-level insulating film 8 is formed. On the first inter-level insulating film 8, a source region 10 and a drain region 12 are formed in a self-aligned manner. A capacitor lower electrode 14 is formed on the side wall structure of the control gate

electrode 6 and the first inter-level insulating film 8 and capacitor upper electrode 16 is disposed so as to sandwich the capacitor lower electrode 14. A second inter-level insulating film 18

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